A Novel Resonant Converter Topology and its Application

Alexander Isurin and Alexander Cook
Vanner Inc. Hilliard, Ohio.

***Abstract*-This paper describes a secondary side resonant converter with particular suitability to step up and high power applications. A description of the basic circuit is followed by a detailed description and some important developments building upon the basic circuit, including inversion and bi-directional configurations. Efficiency is very good (≈94%) as a result of the zero voltage switching and zero current switching operation, and this is demonstrated with test data for two prototype configurations from 1kW to 6kW.**

I. INTRODUCTION

While there are many applications for step up converters, it is difficult to achieve high efficiency, regulate the output over a wide input range, and achieve voltage step up at the same time. This paper describes the development of a power conversion topology from the basic circuits, which is well suited to achieving those goals, the performance features are described, and further applications and variants of the basic topology are shown. Test data is shown for some of the configurations, and measured waveforms are used to demonstrate the operation of the circuit.

II. BACKGROUND

A DC-DC step-up voltage conversion with Vout / Vin>10 and power >1kW can be done by conventional methods, but generally, there is a problem of converting the low voltage into a high voltage without significant losses in efficiency. The efficiency is typically rather low (85%) or the schematic design is very complex (e.g. parallel connection of many low power converters) [1], [2]. When high power applications are involved (i.e., P > 1kw, Vin = 12VDC, Vout = 400VDC) there are even more problems in achieving the conversion with high efficiency and low cost. It is partially attributed to high primary side currents (e.g. > 100A for this case) and a high turns ratio is required in the power transformer. Moreover, there is the problem with EMI, which should be considered in these applications. All the above problems make it difficult to increase the conversion frequency (i.e., usually it is below 50kHZ for powers > 1kW).

The new technology described here provides voltage multiplication in the rectifier stage so the ratio of the power transformer will be half that of a conventional converter. This provides higher efficiency and allows the use of a cheaper transformer. This type of converter only has conduction losses, with commutation losses being negligible. The leakage inductance of the transformer can be used as the inductor of the resonant circuit. The voltage across the reactive components is lower than that of other topologies such as [3], [4], [5], [6], which results in a smaller size for these parts. Changing the commutation frequency of the circuit controls the output for the basic configuration.

One of the major advantages of the present topology lies in the uniformly forward direction of the energy flow. Since energy conversion is unidirectional, there is no time loss on energy transfer, which the bi-directional resonant method inevitably has, as surplus resonant energy is returned to the supply, and this in turn provides a decrease in transformer and conduction losses. There are additional savings in conduction loss arising from the reduced peak forward currents and the absence of loss during the return conduction period. The unidirectional method of energy conversion provides an opportunity for the switches to conduct in the forward direction for 95% of the period, obvious benefits in efficiency particularly at low input voltage and high currents.

III. BASIC CIRCUITS

Looking at the circuit shown in fig. 1, the primary is a full bridge circuit, S1, S2, S3, and S4, with the legs operating 180° apart and with a small dead time between the upper and lower switches to allow for the commutation time. Diodes D1 and D2 form the rectifier, and L_{res} in series with the parallel combination of C_{res1} and C_{res2} forms the resonant tank. Hence the resonance occurs on the secondary side. Commutation of the primary devices is done by magnetising current, built up in the transformer, which charges and discharges the capacitance of the devices and some additional capacitance, which is used to narrow the variation of the commutation time due to device tolerance, and allow more time for turning off the primary side transistors.

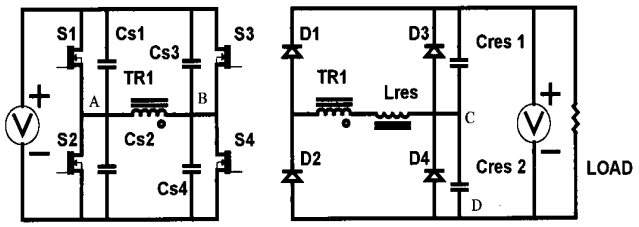

Fig. 1. Basic circuit

For the purposes of understanding the resonant circuit the output voltage can be considered constant, and the ripple on the output capacitor can be ignored and viewed as a voltage source V, so C_{res1} and C_{res2} are being charged and discharged

in an equal and opposite fashion. When for example S1 and S4 are turned on a voltage is applied across L_{res} which is the difference between V_{C1} and V_{in} multiplied by the transformer turns ratio, so the current ramps up and begins charging C_{res1}, and discharging C_{res2}, until the voltage across L_{res} reverses and decays the current to zero. Since the $L_{res}/C_{res1}/C_{res2}$ circuit is a reactive circuit, the wave shape is sinusoidal. At this point the primary devices switch and the process starts again, after commutation of the primary circuit, this time charging C_{res2}. This process can be seen in fig. 2, which is a representation of the voltage A-B (upper waveform), the inductor current, I_{res} (middle waveform), and the secondary voltage C-D (the lower sinusoidal waveform). These waveforms represent operation at maximum frequency and maximum load.

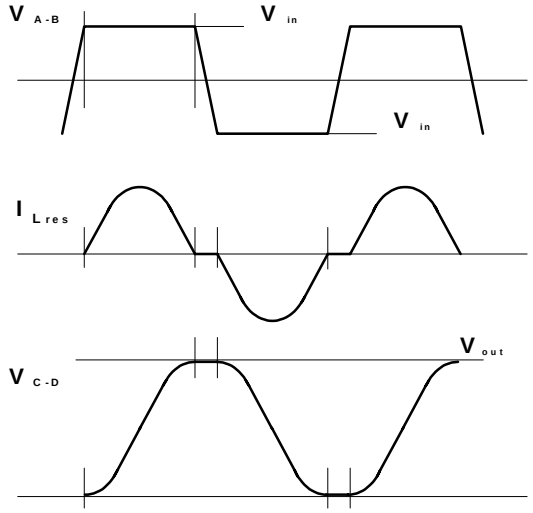

Fig. 2. Voltage and current waveforms.

The operating frequency is set slightly lower than the resonant frequency of the tank, to ensure that the load current has decayed to zero before switching the primary devices. The lower operating frequency is evidenced by the short flat periods of the otherwise sinusoidal transformer current. At the switching instant the device channel current, which is at this time only the transformer magnetising current, is diverted to the node A and node B capacitance. Charging of the node capacitance causes the edges of the trapezoidal waveform, and so the primary devices are zero voltage, low current switched.

IV. Rectifier control

If we now look at fig. 3, we have added an additional switch, formed by S5, S6, D5, and D6, and a couple of small capacitors, C_{res3} and C_{res4}, to the previous circuit, this switch is bi-directional, as we will see later. If S5 and S6 are turned on the operating mechanism is the same as described above, C_{res1} is charged through L_{res} in resonant fashion on the first half of the commutation cycle and C_{res2} is charged during the second half of the conversion cycle. However when S5 and S6 are turned off during the charge cycle, the full output voltage, less the reflected primary voltage, is imposed across the resonant inductor L_{res} because the rectifier is now a full bridge, this causes the inductor current to immediately begin to decay linearly. The regulation of S5 and S6 is conventional PWM, which makes control easy; this is the primary method of regulation for this topology. The devices start each half cycle in the "on" state and are turned off when it is desired to begin termination of the energy transfer. Obviously with PWM control alone the minimum steady state output voltage is governed by the input voltage multiplied by the transformer turns ratio.

The current and voltage waveforms from the new circuit are shown in fig. 4.

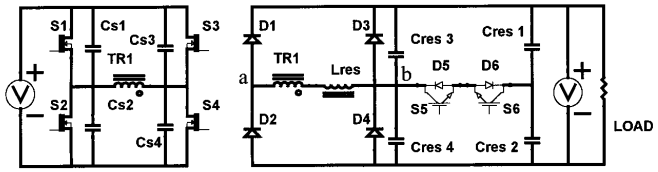

Fig. 3 Converter with secondary side regulation

V. Detailed circuit description

We can look at fig. 4 and fig. 5(a) to fig. 5(g) to see the various time segment circuits and the voltage and current waveforms during PWM operation. The behaviour of the circuit will be described as though there are separate gate drives for S5 and S6. S5 is turned on synchronously with S2 and S3. S6 is turned on synchronously with S1 and S4.

Starting with figure 5(a), which is time segment t_0 to t_1, the secondary side switch is open circuit and the primary side devices S2 and S3 have just begun conduction. The voltage applied to t_1 appears at the secondary across L_{res} and C_{res4}, causing the current in L_{res} to increase and the voltage across C_{res4} to also increase until S6 is forward biased at t_1. The exact timing of this phase depends upon the relative speed of the transitions of the primary devices and the secondary node capacitance at the junction of S5, C_{res4}, and C_{res5}. This is because the secondary node will begin to transition at the same time that the primary side starts to commutate. To keep the drive signals simple, and the efficiency high, we would like the primary device commutation complete before the secondary switch becomes forward biased.

From t_1 to t_2 (figure 5(b)) the complete resonant circuit is in play because S5 is on and D6 is forward biased. This is the main power transfer phase and the resonant ring between L_{res} and $C_{res1}//C_{res2}//C_{res3}//C_{res4}$ can be seen in the shape of L_{res} current and continues until t_2 at which point S5 is turned off,

interrupting the current flowing into C_{res1} and C_{res2} The current is high at this point but the voltage across S5 is zero since the current diverts into C_{res3} and C_{res4}.

From t_2 to t_3 (figure 5(c)) the current in L_{res} charges the node of C_{res3} and C_{res4} until D3 becomes forward biased. This occurs quickly because C_{res3} and C_{res4} are small; their function is purely to allow low switching losses in S5 and S6.

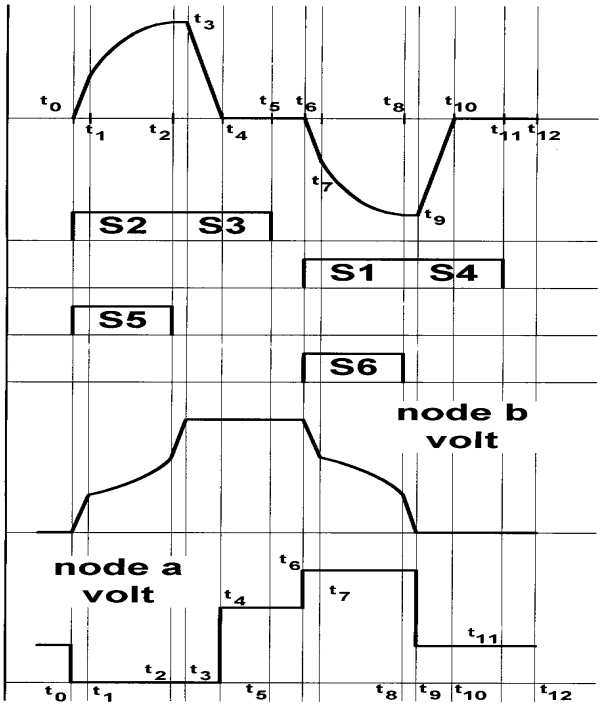

Fig. 4. Basic waveforms, Inductor current (top), gate drive waveforms, rectifier voltage waveforms (lower two).

From t_3 to t_4 the current in L_{res} decays linearly as the voltage across it is clamped between the reflected primary voltage and the output voltage (figure 5(d)). This gives a constant voltage and a constant dI/dt.

When the L_{res} current has decayed to zero the voltage across L_{res} collapses and disconnects the secondary circuit. This starts the t_4 to t_5 period (figure 5(e)). During this time the residual energy in the parasitic components of the secondary can ring. The primary magnetising current does continue to build during this time.

At t_5 the primary side switches are turned off and the commutation of the voltage begins. From t_5 to t_6 (figure 5(f)) the magnetising current in TR1 charges the S1/S2 and S3/S4 node capacitance which is the combination of device parasitic capacitance and C_{s1}, C_{s2}, C_{s3}, and C_{s4}. The secondary side voltage across TR1 tracks this change, so the parasitic capacitance of D1 and D2 in series with L_{res} and C_{res3}// C_{res4} are also across the primary circuit. Part way through the commutation the secondary side voltage forward biases D1 and voltage begins rising across L_{res}, putting L_{res} in series with C_{res3}// C_{res4} and the combination across the TR1 primary. Because of the relatively short times involved this does not significantly impact completion of the primary side commutation.

The circuit now transitions to figure 5(g) to complete the cycle. The timing of the transition at t_6 depends upon the operating point of the circuit. Once it is completed the symmetry of the circuit repeats the performance with voltages and currents inverted, and swapping S6, D5, S1, S4, and D1 for S5, D6, S2, S3, and D2.

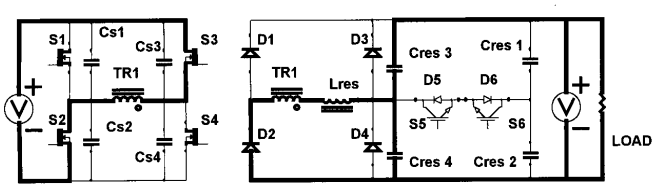

Figure 5(a), t_0 to t_1

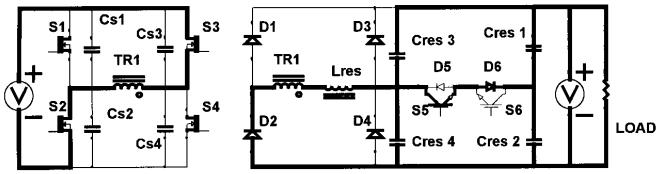

Figure 5(b) t_1 to t_2

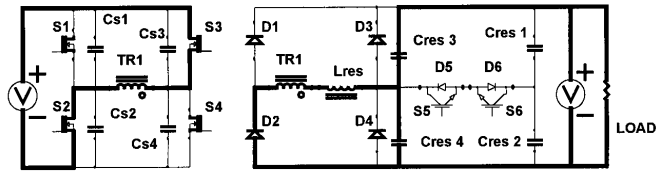

Figure 5(c) t_2 to t_3

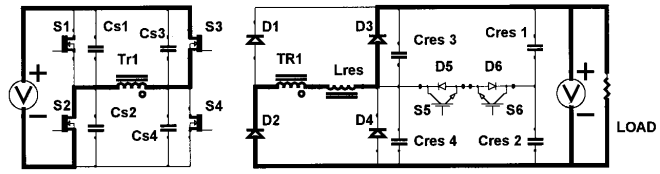

Figure 5(d) t_3 to t_4

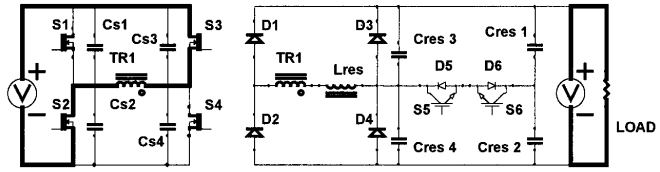

Figure 5(e) t_4 to t_5

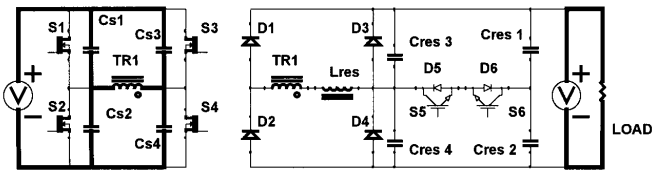

Figure 5(f) t_5 to t_6

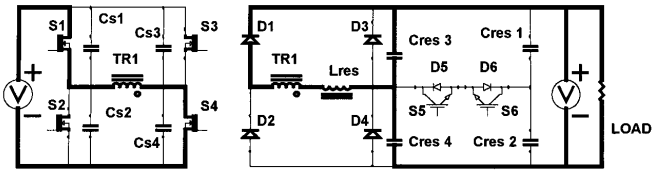

Fig. 5(g) t_6 to t_7

Fig. 6 and fig. 7 are scope traces taken from a breadboard converter operating at about 1kW, it is interesting to compare the actual performance with the theoretical behaviour. The upper trace of both figures shows the transformer output current. The lower trace of fig. 6 shows the voltage at node a (of fig. 3), and the lower trace of fig. 7 shows the voltage waveform at node b (of fig. 3). As soon as the conversion cycle starts the voltage rises in proportion to the transformer primary voltage as the primary side devices commutate (t_0 to t_1), this is easily seen on the lower waveform of both figures as the rapid rise in voltage of node a and fall in voltage of node b up until the point at which the secondary side switch conducts (t_1) and the major portion of the secondary side capacitance (C_{res1} and C_{res2}) comes into play, the commutation, as mentioned before takes a little beyond t_1 to complete. At the same time the resonant rise in current begins (upper trace) until the secondary side devices are turned off (t_2). At that time the transformer current diverts to C_{res3} and C_{res4}, since they are relatively small the voltage rises rapidly until the diode, D3, conducts (at t_3) and the ramp down of L_{res} current begins. This is when the current is seen to decay in a straight line to zero (t_4).

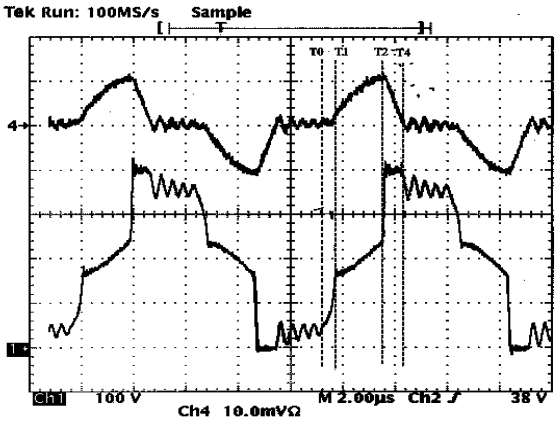

Fig. 6. Transformer output current, and "node a" voltage.

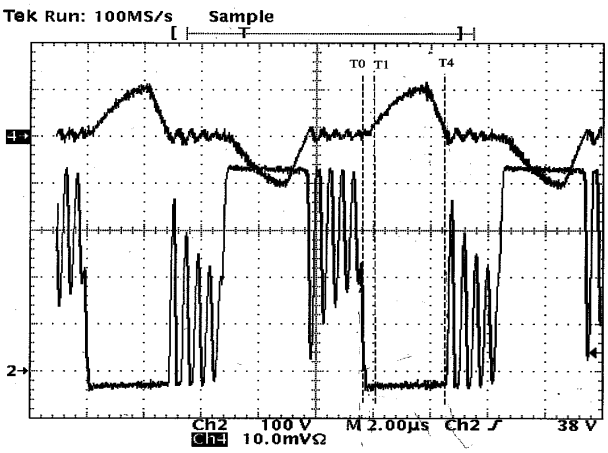

Fig. 7. Transformer output current, and "node b" voltage.

The voltage at node b remains high through both of these intervals and only when the secondary side current has decayed to zero does the voltage drop, at this time the circuit is controlled by the parasitic capacitance of the circuit, and so there is some ringing as the residual energy bounces around. The ringing was aggravated in this case by the transformer construction, it was built with components at hand. The ringing is visible on both voltage traces in fig. 6 and fig. 7.

These segments closely match the predictions although the short time periods t_0 to t_1 and t_2 to t_3 cannot really be seen in detail on the current waveform.

At the end of the first half of the conversion cycle when the primary side devices, S2 and S3, are turned off, the magnetising current from TR1 is diverted to the node capacitance, causing the voltage to rise on S2 and fall on S4, until the body diodes of S1 and S4 conduct. S1 and S4 are then turned on holding the voltage across TR1. As this is occurring on the primary side of TR1 the reflected voltage on the secondary side is also rising, causing L_{res} current to build up in a direction to charge C_{res2}, and the cycle continues, repeating the previous half cycle, but with opposite polarity.

Switching the rectifier in this fashion instead of operating with a variable frequency allows a higher conduction duty cycle for the primary transistors, the transformer, and the rectifier diodes. This is because the resonant tank current is reduced by early termination of the conduction cycle when the secondary side switch turns off. With a lower peak current the conduction time increases reducing the RMS current; this is a significant help to the conversion efficiency. Since the gain change from half wave to full wave rectification is two, we can also see that the basic regulation range will be two to one, less the load regulation of the circuit.

To achieve soft start with this circuit it is recommended variable frequency control be used during ramp up. This is

because it is not possible to bring the output down to zero using PWM control. Control over the output circuit design, and making the circuit strong enough to withstand the start up transient are obvious alternatives, and we have done both successfully.

Fig. 8 shows circuit operation at full load. The traces are the same points as shown in fig. 6 and fig. 7. This is the waveform that would be seen when using a frequency shift control, without the rectifier switch.

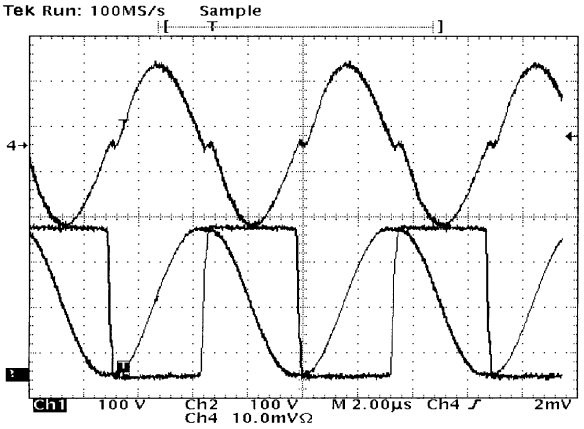

Fig. 8. Transformer output current, "node a", and "node b" voltages, recorded at 1.6kW output power, Vin at 10.5V, and Vout at 321V.

VI. DESIGN CALCULATIONS

Engineering calculation of the resonance circuit in the proposed resonance converter is done regardless the type of the output voltage regulation (i.e., variable frequency or PWM) upon the predetermined minimum input voltage and maximum output power, which determines the L and C values, [3], [4], [7], [8].

First, we calculate C_{res}, (the sum of C_{res1}, C_{res2}, C_{res3} and C_{res4})

$$C_{res} = \frac{P_{\max}}{V_{out}^2 * f_{com}} \quad (1)$$

where P_{max} = maximum output power
V_{out} = output voltage
f_{com} = maximum commutation frequency

Next, we calculate the required transformer turns ratio N:

$$N = \frac{\pi * V_{out}}{4 * \sqrt{2} * V_{in}}$$

Note that this is an ideal approximation and must be modified to compensate for primary and secondary resistive drops.

Then, we calculate resonant frequency of the tank circuit:

$$\frac{1}{f_{res}} = \frac{1}{f_{com}} - 2T_d \quad (3)$$

where f_{res} = resonant frequency
T_d = dead time
f_{com}= desired operating frequency

Now we calculate the inductance for the resonant circuit:

$$L_{res} = \frac{1}{(2\pi f_{res})^2 * C_{res}} \quad (4)$$

where L_{res} is the sum of the TR1 leakage inductance and any discrete inductance required to make up the required value. Now we can calculate the maximum value of the peak switch current at minimum input voltage:

$$\text{Then } I_p = \frac{V_{in}}{Z * N^2} \quad (5)$$

where Z is the characteristic impedance given by:

$$Z = \sqrt{\frac{L_{res}}{C_{res}}} \quad (6)$$

Also, the secondary side current (I_{rms}) will be given by:

$$I_{rms} = 2.5 * I_{out} / 2.8 \quad (7)$$

Where I_{out} = load current

The next stage is the calculation of the power transformer and the determination of the leakage inductance. Leakage inductance will be included in the inductance of the resonance circuit, and with appropriate design, can eliminate the need for an additional discrete inductor. At this stage, we should pay attention to the quality factor of the leakage inductance at the resonant frequency. If its value is lower than 7 we must use an external inductance to get high efficiency and adequate regulation. In this case, the whole calculation is repeated. The desired total quality factor is 10 or more. When the efficiency is calculated only active losses are considered, i.e., conductance losses in switches, diodes, and magnetic components. The built prototypes confirmed the feasibility of the proposed engineering calculations.

VII. OPERATION IN AN INVERTER

The circuit shown in fig. 9 is an inverter with bi-directional capability. The inverter is a typical full bridge and will not be described here. We have tested this configuration with both a stiff DC link (large DC link capacitors), and a weak link (small DC link capacitors).

When operated with small DC link capacitors (weak link), any reactive energy flowing in the load circuit is circulated

back to the battery in between forward energy conversion cycles. So during parts of the cycle the waveform will be controlled by the reverse energy flow. There are numerous control methods that can be used to achieve this. The major benefit of the "weak link" inverter is a reduction in cost for the DC link capacitor, the price is a more difficult controls design and a greater RMS current in the DC converter devices, because they now carry a sinusoidaly weighted current.

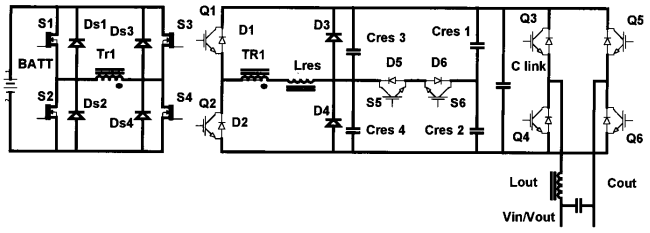

Fig. 9, Bi-directional inverter, with DC link.

Operation with a large DC link capacitor allows reactive energy to be handled within the inverter stage, this eases the performance requirements of the controller, since active waveform control is less important.

The DC converter circuit is operated as a series resonant converter when running in reverse, with Q1 and Q2 being the controlling switches, and S1 to S4 operating as synchronous rectifiers.

VIII. TEST DATA

All of the described configurations of the converter have been tested and efficiency data from several of the DC to DC variants are listed in table 1. The topology for each row of data is shown in the figure listed in the first column of each row.

Table 1, conversion efficiency

Fig.	Vin	Vout	Power out	Efficiency
1	10.4	341	1340	.9
1	10.8	368	1008	.93
1	13.5	457	1559	.93
1	13.7	466	1063	.94
3	11.4	390	970	.94
3	12.3	395	1102	.94
3	13.8	400	1004	.946
3	14.4	405	1208	.934
3	16.6	413	1180	.92
3	41.4	397	4445	.956
3	59.4	404	4560	.927
3	42.2	396	6020	.935
3	61.4	401	6142	.93

IX. CONCLUSION

This paper has presented a very practical conversion topology, which has a high efficiency because all switches are soft switched, and only one switch interrupts significant current. The soft switching behaviour, and low RMS currents, makes the circuit beneficial in high power applications. Its strengths play well into the difficult step up applications. Two particularly interesting variants were also shown: a bi-directional converter, and an inverter.

Looking at the reduction in stress for the power components, we have estimated that cost savings of at least 10% should be realised, when compared with a more conventional circuit.

A patent covering the novel features of this topology has been applied for.

REFERENCES

[1] D. Garabandic, W. G. Dunford, M. Edmunds, Zero-voltage-current switching in high output voltage full-bridge PWM converters using the interwinding capacitance, *IEEE Transactions on Power Electronics, 14 (2)*, 343-349, 1999.

[2] H. Li, F.Z. Peng, J. Lawler, Modeling, simulation, and experimental verification of soft-switched bi-directional dc-dc converters, *IEEE APEC 2001, vol. 2*, 736-744.

[3] M. K. Kazimierczuk and D. Czarkowski, Resonant Power Conversion. New York: John Wiley & Sons, Inc., 1995.

[4] Brown, Power Supply Cookbook. Boston: Butterworth-Heinemann, 1994.

[5] Patent 4,855,888 US Aug. 8,1989 Constant frequency resonant power converter with zero voltage switching

[6] Patent 5,157,593 US Oct.20, 1992 Constant frequency resonant DC/DC converter

[7] I. Batarseh, Resonant converter topologies with three and four energy storage elements, *IEEE Transactions on Power Electronics, 9 (1)*, 64-73, 1994.

[8] S. N. Raju and S. Doralda, An LCL resonant converter with PWM control analysis, simulation, and implementation, *IEEE Transactions on Power Electronics, 10 (2)*, 164-173, 1995.