A Large MOSFET and IGBT Lossless Gate Driver for High-Frequency commutation

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MOSFET and IGBT gate control is achieved by charging and discharging the input capacitance of the device. When we use a relatively simple charge and discharge circuit all of the energy received by the capacitor is dissipated in the passive and active components of the circuit. This may be acceptable when the value of the capacitance is low, e.g. 2 nF - 5 nF, maximum value of charge and discharge current does not exceed 4 A [5]. When a conventional driver is used, the power dissipation in the driver is approximately 1 W or higher, with a commutation frequency 1MHz [4,5,6].

There are many schematic solutions that efficiently work in the above modes. In those cases, efficiency does not go above 80% [5] or the circuit is complicated [2,5,9,13,14], or the voltage at the MOSFET and IGBT gate varies greatly [6,8]. Moreover, there is still a problem in cases where the capacitance value is 50 nF - 100 nF or more, and the commutation frequency is 100 kHz or more. The charge and discharge current goes up to 10 amps and reactive power will be 2-3 VA or higher. In those cases, the power dissipation and the unit size increase. Applying circuits with resonant power exchange can ease this problem. However, they have significant disadvantages. If high efficiency is achieved, the circuit becomes relatively complex. If efficiency is not paramount and the circuit is relatively simple, then the waveform of the charge and discharge gate capacitance takes a sinusoidal form. In this case, requirements for the quality factor of the system become higher, otherwise efficiency suffers.

The proposed topology has a high efficiency, relatively simple circuit and the charge and discharge capacitor waveform is approximately linear. In addition, the charge and discharge times are short, i.e., 80-120 nS. The design is cost effective and is patent pending.

The basic idea of this gate drive is regeneration of energy. The energy that the MOSFET or IGBT input capacitor receives is returned to the source. The topology (Fig.1) consists of: two switches (S1 & S2), a regenerative transformer Tr, a full bridge rectifier (D1-D4), large supply capacitor C_b, antispike diodes (D5 - D6) and the capacitor C_f (the input capacitance of the MOSFET or IGBT).

Fig 2 shows the charging circuit for the capacitor C_f. With the switch S1 turned on, the charge current flows in the circuit +Vcc > S1 > Tr >C_f. This process starts at the time of t_0 (Fig. 6). Between time t_0 and t_1 the secondary winding of the transformer is shunting the primary winding. This way the resonant circuit (the leakage inductance Lr of Tr and C_f) provides the dv/dt for the capacitance C_f. Also, in this time period, the current from the primary winding is coupled into the secondary and it charges C_b, i.e. we have circulating energy. At t_1, the circulating current process stops and C_f has a voltage equal to +Vcc. After t_1 the magnetizing inductance Lm of Tr begins discharging (Fig 3). The current flows from +Vcc > S1 > Tr > D5 > +Vcc until t_2, when current flow stops. Finally, C_f has a voltage of Vcc + Vd.

Looking at the circuit in Fig.4 we now begin the turn off part the cycle at t_3 C_f starts discharging. The discharge current of C_f flows in the circuit C_f > Tr > S2 > -Vcc. Between t_3 and t_4 we have a regeneration process (Fig 6). Most of the energy from C_f returns to C_b. During this time

transformer operates in the same way as in t_0 to t_1. At t_4 the voltage of C_f is equal to zero and the discharge of the magnetizing inductance Lm begins . The current flow is -Vcc > D6 > Tr > S2 > -Vcc (Fig.5). Finally, C_f has a voltage of -Vd. All energy loss in this topology comes from the conductance losses in S1, S2, D1 through D6 and the transformer since there is a soft switch commutation.

An important component of the proposed topology is the transformer. It should have as small as possible leakage inductance since it determines the rise and fall time. The transformer can be a "toroid" where the primary winding of the transformer has one turn or planar, where the primary winding has one turn, (the transformer being a part of the PCB). It is possible to use a **PCB coreless transformer** or any other kind of a transformer that meets the specific technical requirements.

This topology was originally designed for an H-bridge power stage with ZVS and ZCS where each switch has eight MOSFETs (FQB140N03L) in parallel, commutation frequency is 150 kHz and fall time does not exceed 100 nS. The system required maximum efficiency in all power levels.

Figure 7 is the schematic of the gate drive as tested, and the test results matched the theoretical predictions very closely. In this schematic, the equivalent capacitance of eight MOSFETs (the number used during test) is 108nF. The commutation frequency is 150 kHz.

The following results were achieved:

Rise time = 100 - 110nS; Fall time = 80 - 90nS; Efficiency = 83.2%.

Fig 8 and 9 represents the waveform at point N1 and at the MOSFETs' gate (N2).

Fig 10 shows the waveform at the MOSFETs' gate (N2).

Fig 11 shows the waveform (N3) of a charge/discharge current of the gate's capacitance (5A/div).

Fig 12 is similar to Fig 11. However, it illustrates the waveform at 1A/div. You can see the discharge of the magnetizing inductance.

Fig13 represents the waveform of the regeneration current (N4).

The following results were achieved:

Rise time - maximum 110 nS, Fall time maximum 100 nS

(commutation time increases when any current probe is introduced in the circuit, without the probes the times are reduced).

The efficiency has been calculated as follows:

1. When there is 12VDC input and a commutation frequency of 150 kHz, current received by the gate driver without MOSFETs is measured at I=26mA
2. When there is 12VDC input and a commutation frequency of 150 kHz, current received by the gate driver with MOSFETs is measured at I=70mA. Also, a peak to peak voltage as measured on the MOSFET gate, Vc=12.72V
3. Calculating the efficiency:

$$\eta = \frac{Ec}{P + Ec} = \frac{2621}{2621 + 528} = 0.832$$

Where:

P - power consumption from the source;

P = 12 x (70 – 26) = 528mW

Ec - energy supplied to and regenerated from, the input capacitance of the MOSFET.

$Ec = Vc^2 \times C_f \times F = 12.72^2 \times 0.108 \times 0.15 = 2.621W = 2621mW$

This topology can be recommended for application in those cases where conversion is carried out by devices with large input capacitance, and the commutation frequency is 100kHz or more. Particularly, this topology can be advantageous in cases where power consumption of the drive becomes of critical importance, such as when low load efficiency is paramount.

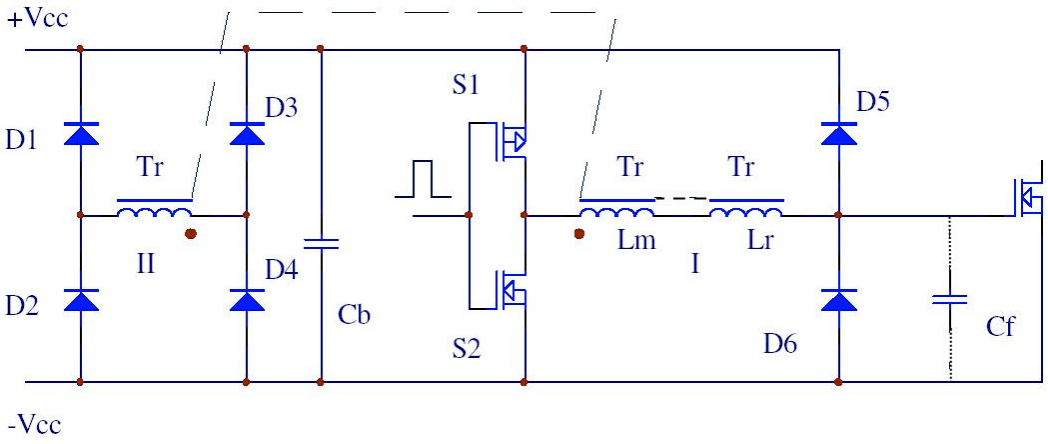


Fig – 1

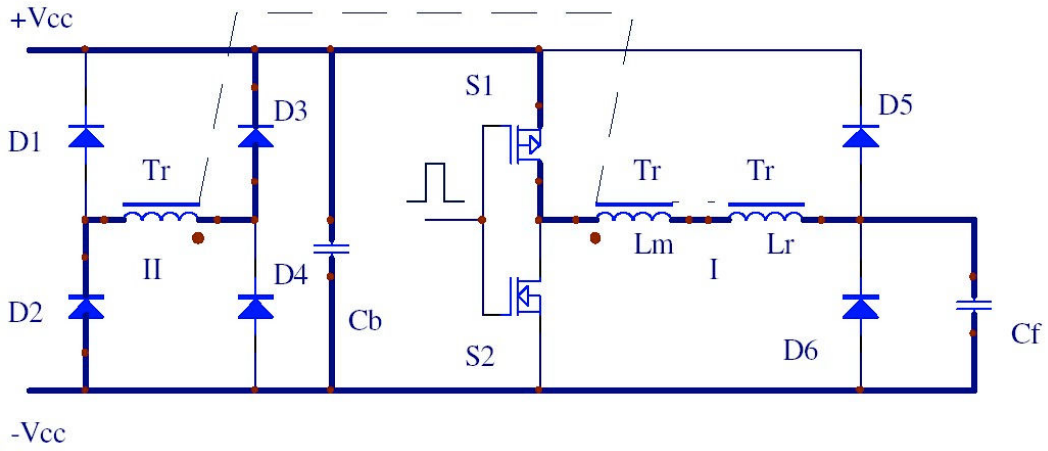


Fig – 2

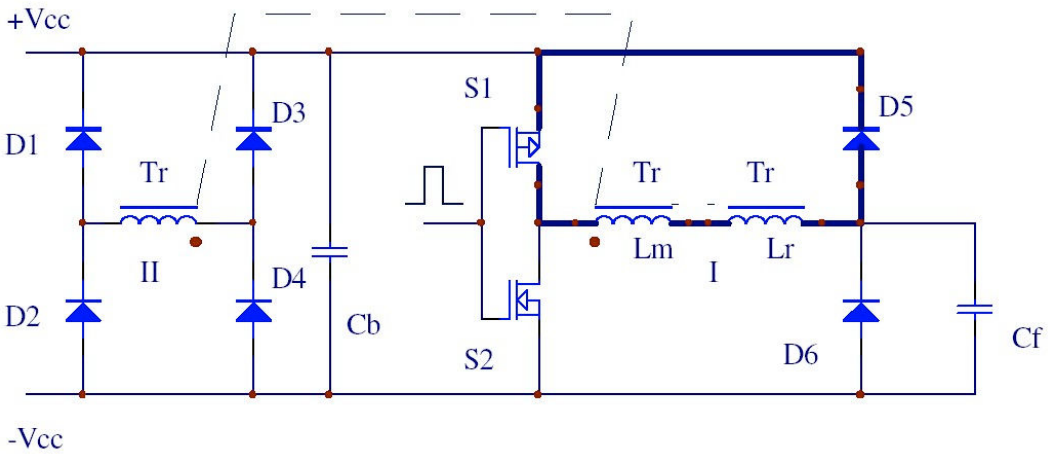


Fig – 3

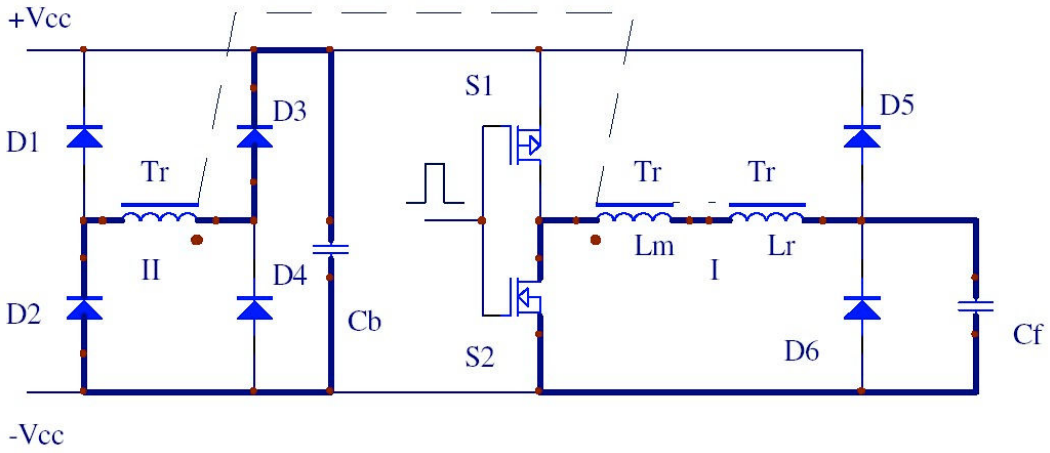


Fig – 4

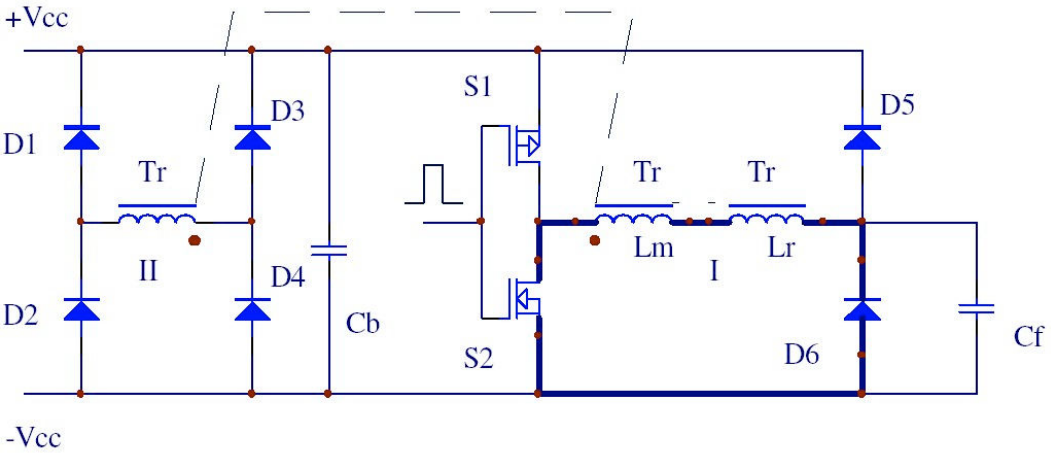


Fig – 5

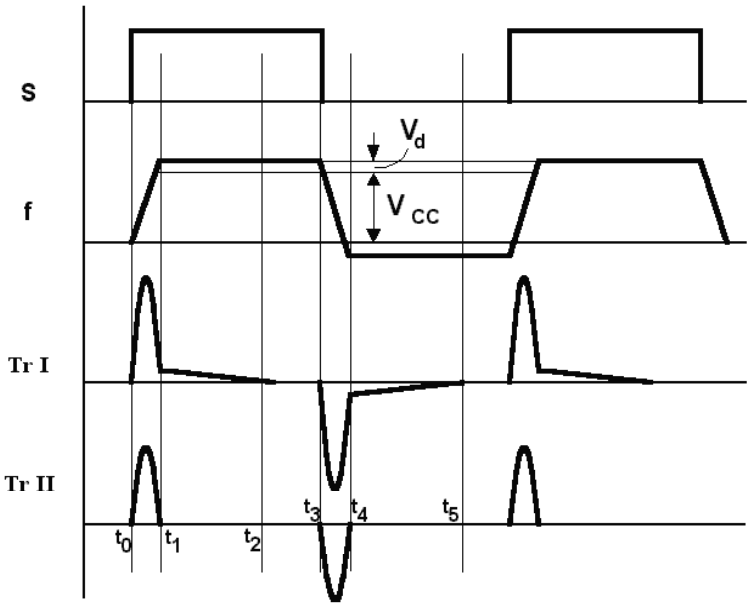


Fig – 6

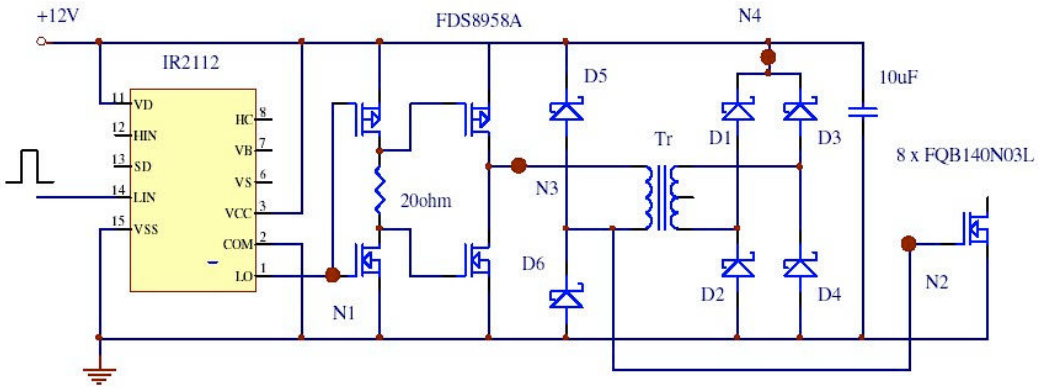


Fig – 7

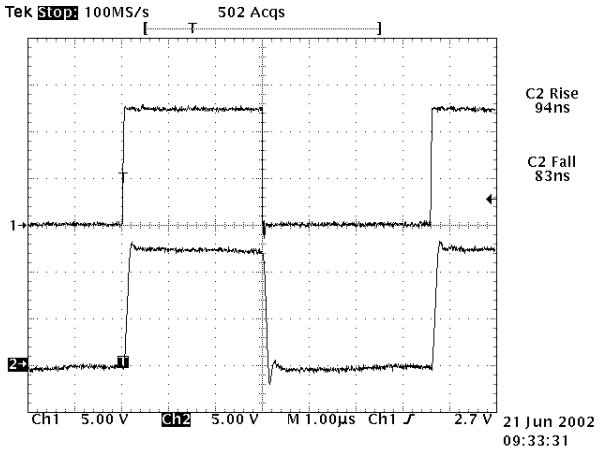


Fig – 8

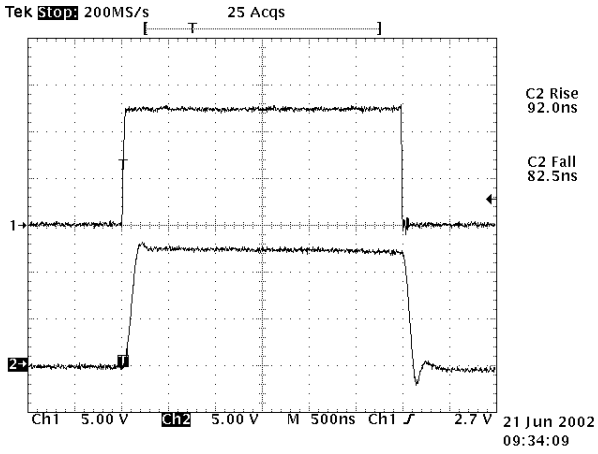
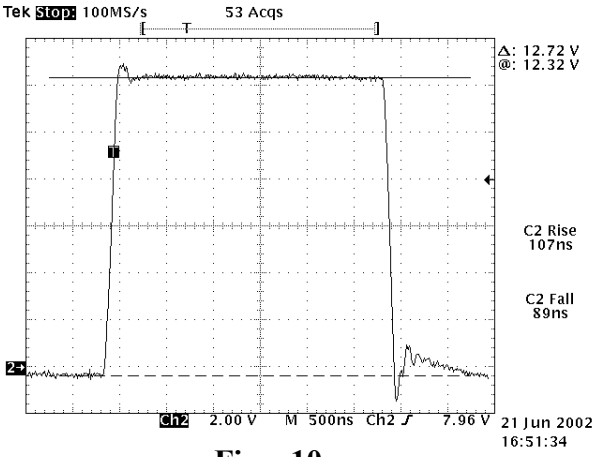


Fig – 9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Δ: 12.72 V
@: 12.32 V
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107ns
C2 Fall
89ns
Ch2 2.00 V M 500ns Ch2 ƒ 7.96 V
21 Jun 2002
16:51:34

Fig – 10

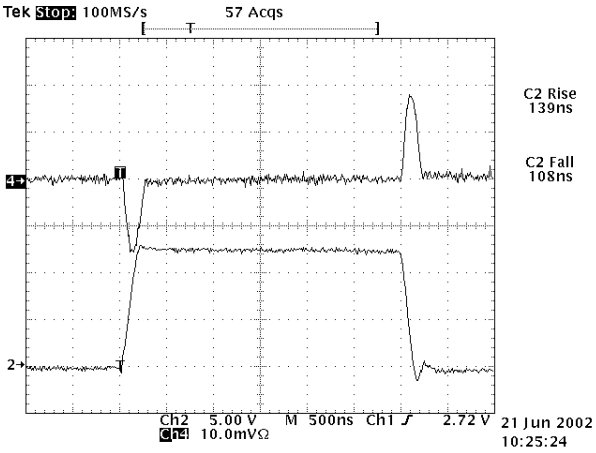
Tek Stop: 100MS/s 57 Acqs
C2 Rise
139ns
C2 Fall
108ns
Ch2 5.00 V M 500ns Ch1 ƒ 2.72 V
Ch1 10.0mVΩ
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Fig – 11

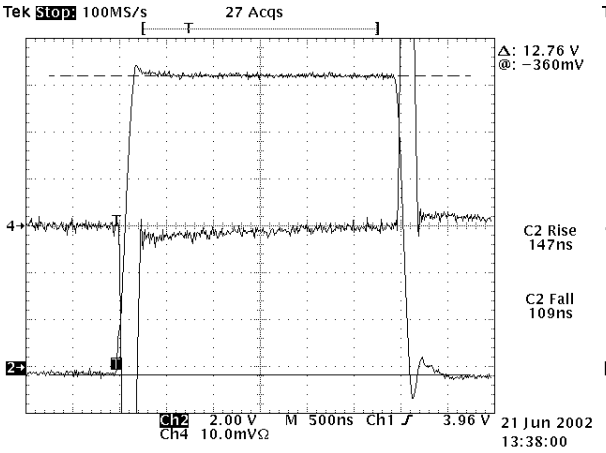

Fig – 12

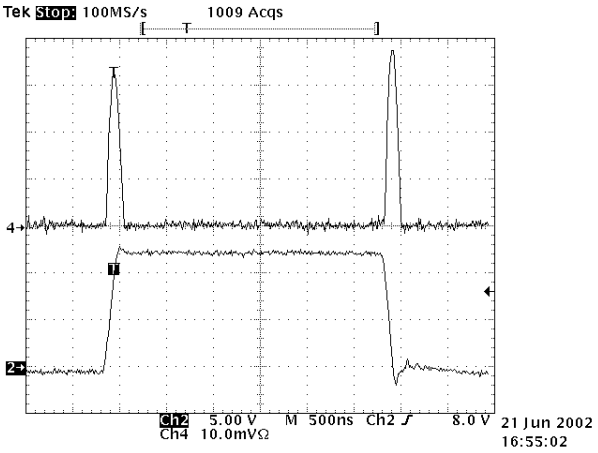

Fig – 13

REFERENCES

[1] D.Maksimovic' "A MOS gate driver with resonant transitions" PESC1991 pp.528-532

[2] S.H.Weinberg "A novel lossless resonant MOSFET driver" PESC1992 pp. 1004-1010

[3] Herman L.N. Wiegman "A resonant pulse gate driver for high frequency applications" APEC 1992 pp.738-737

[4] J.Diaz, M.A.Perez, F.M.Linera, Aldana F."A new lossless power MOSFET driver based on simple DC/DC converters" PESC1995 pp.37-43

[5] Kaiwei Yao, Fred C.Lee "A novel resonant gate driver for high frequency synchronous buck converter" APEC 2001

[6] Ian D. de Vries "A resonant power MOSFET / IGBT gate driver" APEC 2002

[7] Wally E.Rippel "Monolithic transistor gate energy recovery system" United States Patent Number 4,873,460 oct.1989

[8] Robert L. Steigerwald “High efficiency gate driver circuit for a high frequency converter “ United States Patent Number 4,967,109 oct.1990

[9] Robert L. Steigerwald “Lossless gate driver circuit for a high frequency converter” United States Patent Number 5,010,261 apr.1991

[10] Eugene T.Perusse “High efficiency FET driver with energy recovery” United States Patent Number 5,134,320 jul.1992

[11] Boris S.Jacobson “High frequency resonant gate driver for a power MOSFET” United States Patent Number 5,264,736 nov.1993

[12] David W.Cripe “High efficiency quasi-square wave drive circuit for switching power amplifiers” United States Patent Number 5,276,357 jan.1994

[13] Simon H.Weinberg “Low-loss resonant circuit for capacitance driver” United States Patent Number 5,537,021 jul.1996

[14] Erich Bayer “Circuit arrangement for driving a MOS Field-effect transistor” United States Patent Number 5,548,240 aug. 1996

[15] Robert L.Kollman “Resonant bilateral charging and discharging circuit” United States Patent Number 5,804,943 sep.1998

[16] David B.Parks “Resonant gate driver” United States Patent Number 6,208,535 mar.2001