High Frequency Step -up DC -DC Converter with High Efficiency for High Power Application and the Principle of its Control.

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ABSTRACT

The paper presents the control strategy for an isolated, step-up, high frequency, DC-DC converter with a high efficiency (approximately 94%), low idle losses (2-4 W), and low cost. All active circuit components work in ZCS and/or ZVS. The principal circuit is a resonant topology, with no energy re-circulation, where control is done by varying commutation frequency from idle to 25-30% load, and by soft-switched PWM at higher loads. This converter was designed as part of an inverter/charger that has been implemented in two prototypes with nominal output powers of 2.2kW and 6kW. The latter has a weak DC- link.

1. Background

This paper presents the control principle for a new DC-DC conversion topology. The presented topology is an isolated step-up resonant converter, with no energy re-circulation, where control in done in the secondary circuit by PWM at heavy loads or by varying the commutation frequency at idle-to 25-30% load.

Voltage conversion with a high step-up ratio (e.g. Vout/Vin >20) and at power levels greater than 1kW can be done by many conventional methods. However those methods either have a low efficiency (85%) [7] or a complex circuit that results in a relatively high cost. In addition, commutation frequency for power levels above 1kW does not go above 50kHz [5,6]. When one faces the task of designing a cheap, high efficiency, isolated step-up DC-DC converter with highly demanding technical requirements (e.g., Pout=2.2kW; Vin=10.5-16VDC; Vout=400VDC; and control to be done over the whole range from idle to full load) the conventional methods become even less feasible.

In particular when the commutation current is relatively high (e.g. 250A), it is a problem to damp spikes, which might lead to a decrease in the commutation frequency and an increase in the size of the magnetic components, and as result, their cost. This problem can be solved by with ZCS technology in high current circuits, using variable frequency regulation. However, another problem arises; when the input voltage is maximum the current stress on the semi-conductors, and the peak flux density in the transformers, are increased. This, in turn, increases the number of semiconductors and the size of the transformer, decreases the efficiency and, as a result, increases the cost.

Moreover, there is the problem with EMI, which should be considered in these applications. All the above problems make it difficult to increase the conversion frequency (i.e., usually it is below 50kHZ for powers > 1kW).

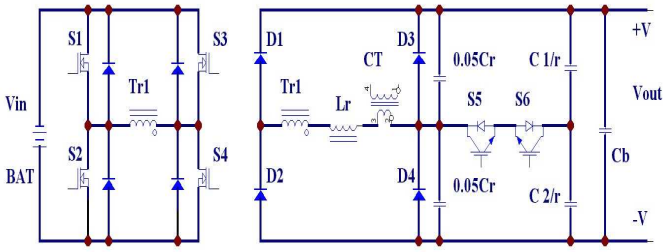

Figure 1 Basic step-up circuit

The present converter (Fig.1) is ideal for step-up applications. It significantly reduces the disadvantages discussed above. Moreover, its efficiency is more than 91% over most of its load range, generally it is 94%, with a peak of 97%, and it has a simple circuit. In addition, for the same specification it has a relative cost lower than that of conventional circuits (10% or more).

This paper evolved from an earlier project, for which a description of the power stage converter can be found in the text of "A Novel Resonant Converter Topology and its Application" [1] and US Patent 6.483.731 [16].

The focus here is on the principle of control for the above topology when it is in the step-up mode. The advantages of the above topology (e.g., ZCS commutation in high current circuits, and the significant decrease in the current stress under high input voltage) can be best realized using this control.

2. Control Strategy

The presented control topology implements the combination of two common methods of control; variable commutation frequency and PWM [3,4,8,9,11,12,13,14,15,17,18].

Figure 2 represents one of the possible variants of how the PWM and the commutation frequency vary for a given drive level. When the converter starts it also follows this ramp up of PWM duty cycle and commutation frequency. As we can see, when the load changes from idle to 25-30% the control is mostly done by the varying commutation frequency. In this case, the PWM minimizes the current stress on the power components with maximum input voltage, which results in higher efficiency. This method of control provides high stability of the converter with light load and low energy consumption at idle (2-4W), which is especially important when the converter runs from a battery. The converter transitions through the variable frequency mode to achieve soft start for the unit.

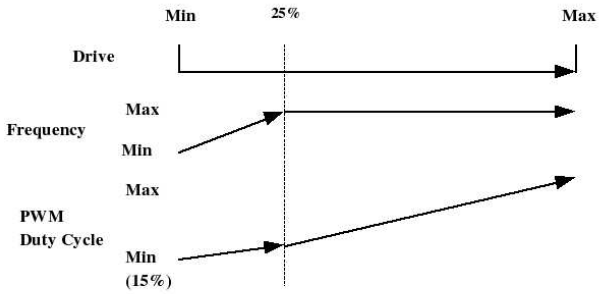

Figure 2

When the commutation frequency reaches its maximum (100kHz or more) control continues by PWM in the secondary circuit. The power stage works in two modes, one is a uni-directional (no energy recirculation) resonant converter with voltage doubling rectification, another provides discharge of the resonant inductor into the load. The active components switching between these two modes are S5 and S6, working under ZVS. The other switching components are operating under both ZCS and ZVS. The combination of the two control methods, i.e. varying the frequency and PWM, provides a high performance converter. Specifically full control of the power with a stable output voltage and high stability with a clean fast response to fast changes in load (from idle to full power and vice versa), yet the input voltage can vary twofold.

3. Waveforms

Figure 3 shows a block diagram of the entire control system in the step-up mode. It has two independent control loops that are interconnected by a synchronization pulse. One loop is for the control of the commutation frequency, the other is for the PWM.

Figure 4 presents the waveforms at various points in the circuit at an intermediate output level (before maximum frequency is reached).

Figures 5, 6, and 7, show power stage modes corresponding to particular times marked on figure 4.

4. Control Circuits

The frequency control loop consists of the following:

The output of the error amplifier drives a voltage to current converter, which, in turn, charges CAP1. When the voltage on CAP1 reaches Vref, comp1 produces a signal that releases the set pin for Flip-Flop F-F1. The first signal that arrives at the clock input of F-F1 toggles its output. This signal triggers timer 2, and timer1, timer 2 discharges CAP1, while the output from the timer 1 providing synchronizes the two control loops. The synchronization pulse also clocks F-F2, which provides the separation of the power stage control pulse into even and odd through the AND gates 3, 4, 7, and 8. The duration of the pulse from timer 1 equals ½ of the minimum commutation period, i.e. the maximum commutation frequency.

The comparator comp3, F-F3, OR2 and the gate AND1 are needed to reduce the duration of the power conversion cycle (to reduce the peak current in the resonant circuit) during initial ramp up (soft start) of the power converter. This is because during that time the output capacitor of the converter is essentially a short circuit (figure 8). The comparator comp5, AND2, and OR1 provide clamping of the primary side converter circuit when there is zero current in the converter secondary circuit (Figure 7). Discreteness of the commutation frequency change depends upon the clock frequency, which should be at least 4 times the maximum commutation frequency of the power stage. The higher the clock frequency, the finer the discreteness of the commutation frequency changes for the power stage. The ultimate commutation frequency change range exceeds 1000:1.

The PWM control loop consists of the following components:

1. The limiter of the maximum/minimum duty cycle of the PWM (D1 and D2). The minimum limit is needed to make the secondary circuit work in the resonance mode at the beginning of the power conversion cycle. The maximum limit provides a higher average output current (and hence a lower RMS current) density during the conversion cycle when at high power. This is because the current drop to zero results from the Lr energy discharge rather than the resonance process, and thus occurs quicker. The minimum duty cycle is around 10%, and the maximum is around 90%.
2. The comparator comp2 and AND5 produce PWM pulses, synchronized by a pulse from timer1 by F-F4 and AND6, and terminated by the charging of CAP2.
3. The comparator comp4, OR2, F-F4, and AND6 provide a current limit for the resonant circuit.

5. Test Data

The DC-DC converter and control we have described made it possible to build an inverter-charger that converts solar energy to AC with nominal output power of 6kW, a crest factor of 5, a maximum commutation frequency of 150kHz, power consumption of 9-10W at idle, and a weak DC-link. Also, an inverter-charger of 2.2kW was built. The results presented in Table 1 are from the DC-DC converter portion of these inverter-chargers.

Vin	Vout	Pout W	Efficiency	Vin	Vout	Pout W	Efficiency
10.5	400	2,200	90%	41.5	400	4500	95.60%
11.5	400	1,500	94.0%	42.2	400	6,000	93.7%
11.8	400	2,200	92.5%	48.0	400	1,800	97.0%
12.5	400	400	97.0%	59.0	400	4,500	93.5%
16.0	400	1,200	92.0%	61.4	400	6,100	93.8%
16.0	400	2,200	91.5%	80.0	400	6,000	93.5%
18.0	400	2,200	91.5%				
Idle power loss 2 watts				Idle power loss 4W			

Table 1 Test data for two prototype converters

6. Summary

The authors suggest that the above presented converter can be ideally used in step-up topologies for high power application where the output voltage is greater than 200VDC. The converter is characterized by good regulation, a fast clean transient response, low device stress, high efficiency, low emissions, and low cost compared to other converters with similar performance goals that our known to the authors. Unfortunately, more detailed information on the present technology cannot be included due to the size limit of the present paper. The analysis of the further development is in process and will be presented later.

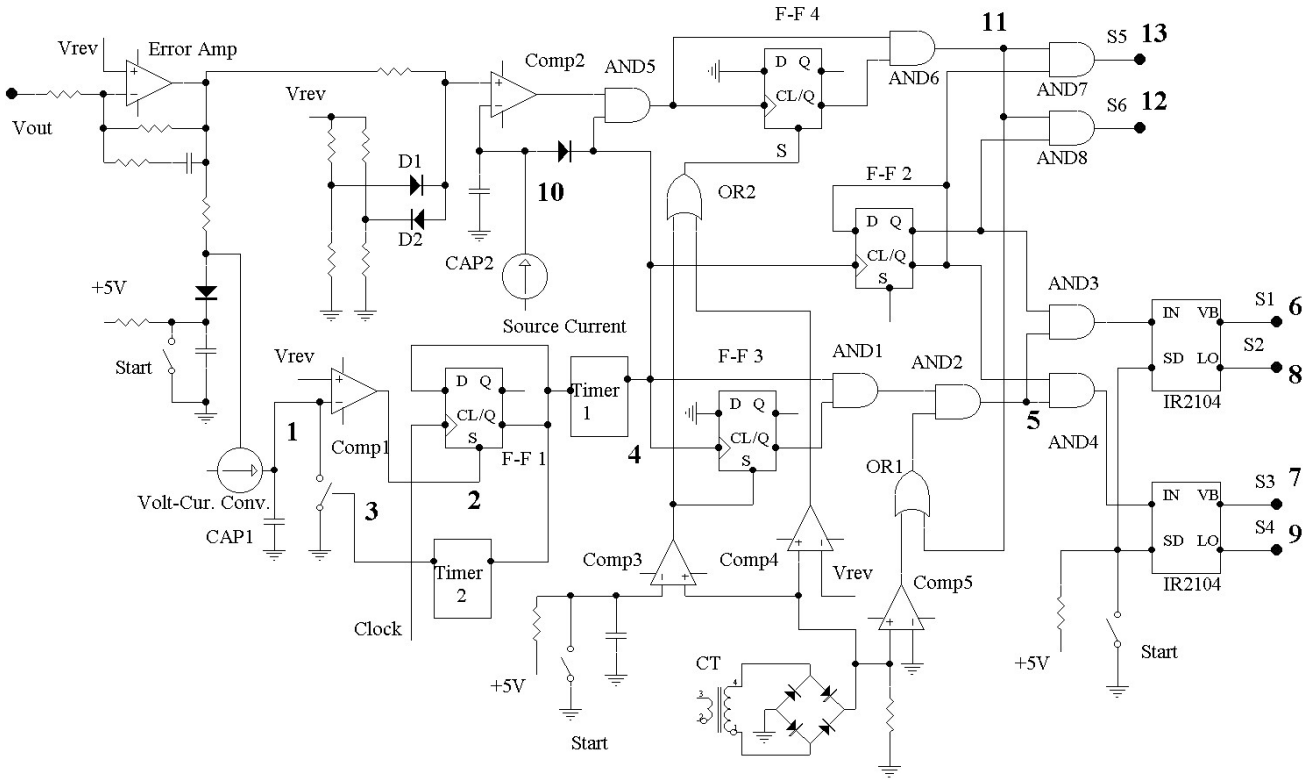

Figure 3 Block diagram of the control system.

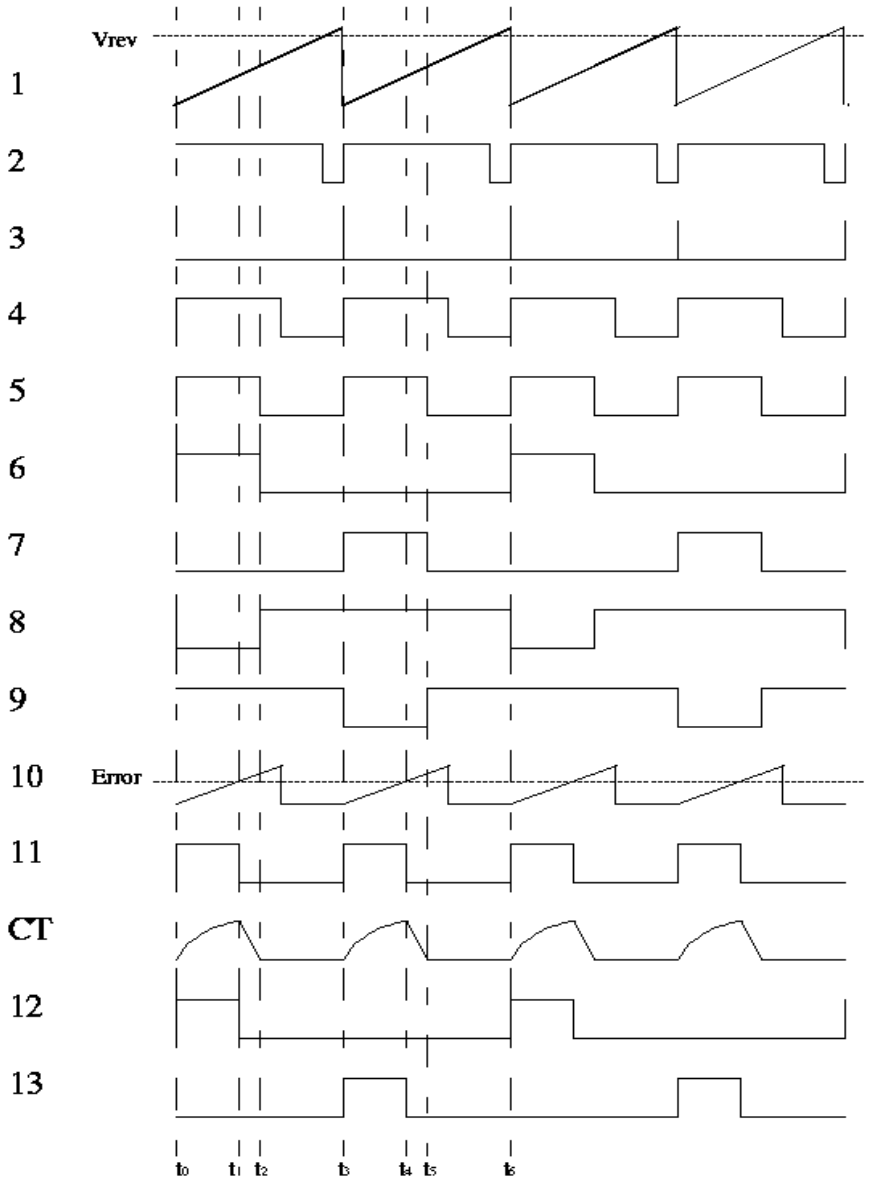

Figure 4 Waveforms

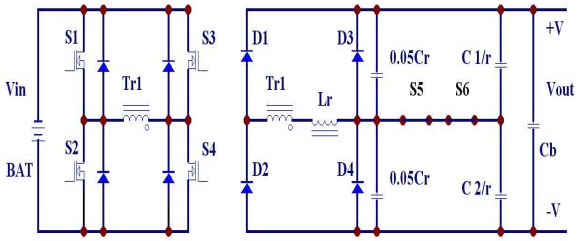

Figure 5 Basic circuit from t0 to t1 and t3 to t4

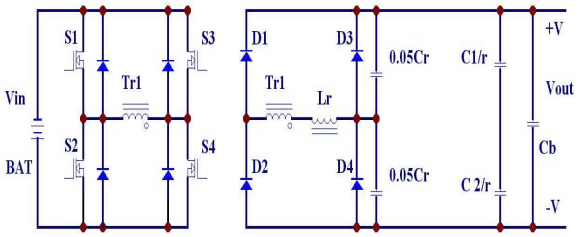

Figure 6 Basic circuit from t1 to t2 and t4 to t5

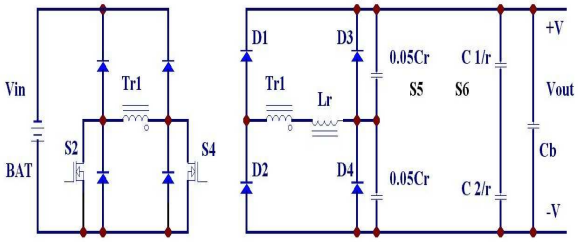

Figure 7 Basic circuit from t2 to t3 and t5 to t6

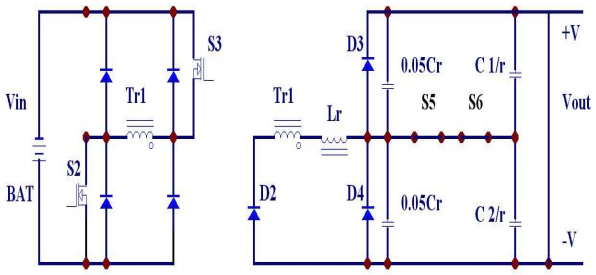

Figure 8 Basic circuit when the converter starts with the first pulse

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